Appl. No. 10/082,822
Amdt. dated September 11, 2003
Reply to Office Action of March 12, 2203,

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

57. (Currently Amended) A method for operating a ~~driver~~ circuit adapted to electrostatically ~~driving~~ drive a MEMS structure, the method comprising:

applying a first voltage to a drive electrode that electrostatically drives the MEMS structure;

generating a first ~~output~~ current in response to a first digital control word; ~~and~~

integrating the first ~~output~~ current to ~~increase or decrease~~ generate a first difference voltage by which the ~~a~~ first voltage ~~by an amount~~ is changed thereby to generate a second voltage, said first digital control word specifying whether said first difference voltage is greater than, smaller than or equal to 0 volts; ~~and in a direction controlled by the first digital control word to obtain a second voltage which can be coupled to a drive electrode that electrostatically drives the MEMS structure.~~

applying the second voltage to the drive electrode that electrostatically drives the MEMS structure;

generating a second ~~output~~ current in response to a second digital control word;

integrating the second ~~output~~ current to ~~increase or decrease the~~ generate a second difference voltage by which the second voltage is changed thereby to generate a third voltage, said second digital control word specifying whether said second difference voltage is greater than, smaller than or equal to 0 volts; ~~by an amount and in a direction controlled by the second digital control word to obtain a third voltage which can be coupled to the drive electrode.~~ and

applying the third voltage to the drive electrode that electrostatically drives MEMS structure, wherein the first voltage is different from the second voltage.

58. (Original) The method of claim 57, wherein the driver circuit fits within a footprint of the MEMS structure to be driven by the driver circuit.

59. (Currently amended) A method for operating a driver circuit that electrostatically drives a MEMS structure, comprising:

generating a first output current in response to a first digital control word; and

integrating the first output current to increase or decrease a first voltage by an amount and in a direction controlled by the first digital control word to obtain a second voltage which can be coupled to a drive electrode that electrostatically drives the MEMS structure; wherein the driver circuit fits within a footprint of the MEMS structure ~~The method of claim 58~~, wherein the footprint is at most 1.2 by 1.2 mm^2.

60. (Original) The method of claim 58, wherein the MEMS structure is a micromirror.

61. (Currently amended) The method of claim 57, wherein the first digital control word includes one or more bits representing an integration duration and said generating the first ~~output~~ current comprises generating the first ~~output~~ current for the integration duration.

62. (Currently amended) The method of claim 61, wherein the first digital control word further includes a bit representing an integration direction and said generating the first ~~output~~ current further comprises generating the first ~~output~~ current in the integration direction.

63. (Currently amended) The method of claim 62, wherein the first digital control word further includes one or more bits representing an integration current level and said generating the first ~~output~~ current further comprises generating the first ~~output~~ current at the integration current level.

64. Canceled

65. (Original) A method for operating a driver circuit that electrostatically drives a MEMS structure, comprising:

receiving a first digital control word including information relating to a first integration duration, a first integration direction, and a first integration current level, the first digital control word representing a change to a first voltage across an integrate-and-hold capacitor;

in response to the first digital control word, generating a first reference current in the first integration direction, at the first integration current level, and for the first integration duration; and

in response to the first reference current, generating a first output current in the first integration direction, at a level scaled relative to the first integration current level, and for the first integration duration;

supplying the first output current to the integrate-and-hold capacitor, wherein a second voltage develops across the integrate-and-hold capacitor and can be coupled to a drive electrode that electrostatically drives the MEMS structure.

66. (Original) The method of claim 65, wherein the driver circuit fits within a footprint of the MEMS structure to be driven by the driver circuit.

67. (Original) The method of claim 66, wherein the structure is a micromirror.

68. (Original) The method of claim 66, further comprising:

receiving a second digital control word including information relating to a second integration duration, a second integration direction, and a second integration current level, the second digital code word representing a change to the second voltage across the integrate-and-hold capacitor;

in response to the second digital control word, generating a second reference current in the second integration direction, at the second integration current level, and for the second integration duration;

in response to the second reference current, generating a second output current in the second integration direction, at a level scaled relative to the second integration current level, and for the second integration duration; and

supplying the second output current to the integrate-and-hold capacitor, wherein a third voltage develops across the integrate-and-hold capacitor and can be coupled to the drive electrode.

69. (Original) The method of claim 65, wherein said generating the first output reference current comprises:

in response to receiving the information relating to the first integration duration, generating an active count signal during the first integration duration;

in response to receiving the active count signal and the information relating to the first integration current level, enabling a combination of output branches in a first current mirror to generate an internal reference current;

in response to receiving the active count signal and the information relating to the integration direction, allowing the enabling of a first plurality of output branches or a second plurality of output branches in a second current mirror, the second current mirror including a reference branch receiving the internal reference current; and

in response to receiving the information relating to the first integration current level, enabling a combination of the output branches of the first or the second plurality of output branches allowed by the active count signal and the information relating to the integration direction to generate the output reference current.

70. (Original) The method of claim 65, wherein said generating the first output current comprises:

supplying the first reference current to a first current mirror, wherein the first current mirror generates an internal reference current scaled relative to the first reference current; and

supplying the internal reference current to a second current mirror, wherein the second current mirror generates the first output current in a down direction scaled relative to the internal reference current.

71. (Original) The method of claim 70, wherein the second current mirror comprises an output branch including a high voltage transistor comprising a source coupled to a high voltage supply.

72. (Original) The method of claim 70, further comprising supplying a small current to the first current mirror when the reference current is zero.

73. (Original) The method of claim 65, wherein said generating the first output current comprises:

supplying the first reference current to a third current mirror, wherein the third current mirror generates a third internal reference current scaled relative to the first reference current;

supplying the first internal reference current to a fourth current mirror, wherein the fourth current mirror generates a fourth internal reference current scaled relative to the first internal reference current; and

supplying the fourth reference current to a fifth current mirror, wherein the fifth current mirror generates the first output current in an up direction scaled relative to the fourth internal reference current.

74. (Original) The method of claim 73, wherein each of the fourth and the fifth current mirrors comprises an output branch including a high voltage transistor having a source coupled to a high voltage supply.

75. (Original) The method of claim 73, further comprising supplying a small current to the third current mirror when the reference current is zero.